EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jia Lu, Reg. No. 61,543 on 13 February 2009.

The claims are amended as follows:

1. A capacitance detection circuit, comprising:

a first buffer amplifier, wherein an input of said first buffer amplifier is connected to a capacitor to be detected ~~via~~ by a signal wire;

a first diode and a second diode, connected in series, the anode of the first diode connected to the cathode of the second diode at a first junction point, and the anode of the second diode connected to the signal wire, and the cathode of the first diode connected to a first power supply;

a third diode and a fourth diode, connected in series, the anode of the third diode connected to the cathode of the fourth diode at a second junction point, and the cathode of the third diode connected to the signal wire, and the anode of the fourth diode connected to a second power supply;

wherein:

an output terminal of the first buffer amplifier is connected to the first junction point of the first diode and the second diode via a first capacitance;

said output terminal of the first buffer amplifier is connected to the second junction point of the third diode and the fourth diode via a second capacitance;

the first junction point is connected to a point having a voltage whose value is between the voltage of the first power supply, and the voltage of the signal wire, via a first resistor;

the second junction point is connected to a point having a voltage whose value is between the voltage of the second power supply and the voltage of the signal wire, via a second resistor.

4. The capacitance detection circuit according to claim ~~3~~ 1,

wherein the first resistor and first ~~capacitor~~ capacitance are components of a high pass filter that passes frequency elements of output signals from the first buffer amplifier ~~unit~~ corresponding to ~~variant~~ varying capacitance of the capacitor to be detected, and AC components of ~~the~~ a bias voltage added to said capacitor to be detected, and

the second resistor and second ~~capacitor~~ capacitance are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier ~~unit~~ corresponding to ~~variant~~ varying capacitance of the capacitor to be detected, and AC components of ~~the~~ a bias voltage added to the said capacitor to be detected.

5. The capacitance detection circuit according to Claim ~~3~~ 1, further comprising:

a second buffer amplifier unit connected between (i) a junction point of the first resistor and the first capacitor and (ii) the first junction point; and

a third buffer amplifier unit connected between (i) a junction point of the second resistor and the second capacitor and (ii) the second junction point.

9. A circuit that detects a capacitance of a capacitor ~~to be detected~~, comprising:

a first buffer amplifier, wherein an input of said first buffer amplifier is connected to the capacitor to be detected ~~via~~ by a signal wire, and wherein the voltage gain of the said first buffer amplifier is unity;

a first diode and a second diode connected in series between the signal wire and a first power supply, connected so that ~~in a way~~ a current flows from the signal wire to the first power supply via the first and second diodes;

a third diode and a fourth diode connected in series between the signal wire and a second power supply, connected so that ~~in a way~~ a current flows from the second power supply to the signal wire via the third and fourth diodes; and

a resistor connected between the signal wire and a voltage that is equal to or lower in value than a voltage of the first power supply and equal to or higher than a voltage of the second power supply,

wherein:

an output terminal of the buffer amplifier ~~unit~~ is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance;

the first junction point is connected to a point having a voltage, the value of which is between the voltage of the first power supply and the voltage of the signal wire, via a first resistor; and

the second junction point is connected to a point having voltage, the value of which is between the voltage of the second power supply and the voltage of the signal wire, via a second resistor.

10. A circuit that detects a capacitance of a capacitor ~~to be detected~~, comprising:

a first buffer amplifier, wherein an input of said first buffer amplifier is connected to the capacitor to be detected ~~via~~ by a signal wire, and wherein the voltage gain of the first buffer amplifier is unity;

a first diode and a second diode connected in series between the signal wire and a first power supply, connected so that ~~in a way~~ a current flows from the signal wire to the first power supply via the first and second diodes;

a third diode and a fourth diode connected in series between the signal wire and a second power supply, connected so that ~~in a way~~ a current flows from the second power supply to the signal wire via the third and fourth diodes; and

a resistor connected between the signal wire and a voltage, the value of which ~~that~~ is equal to or lower in value than a voltage of the first power supply and equal to or higher than a voltage of the second power supply,

a capacitor connected between an output terminal of the first buffer amplifier ~~unit~~ and a first junction point of the first diode and the second diode;

a resistor connected to the first junction point and to a point ~~having~~ maintained at a voltage, the value of which is between the voltage of the first power supply and the voltage of the signal wire;

a capacitor connected between the output terminal of the first buffer amplifier ~~unit~~ and a second junction point of the third diode and the fourth diode; and

a resistor connected to the second junction point and to a point ~~having~~ maintained at a voltage, the value of which is between the voltage of the second power supply and the voltage of the signal wire.

11. A circuit that detects a capacitance of a capacitor ~~to be detected~~, comprising:

a first buffer amplifier, wherein an input of said first buffer amplifier is connected to the capacitor to be detected ~~via~~ by a signal wire, and wherein the voltage gain of the first buffer amplifier is unity;

a first diode and a second diode connected in series between the signal wire and a first power supply, connected so that ~~in a way~~ a current flows from the signal wire to the first power supply via the first and second diodes;

a third diode and a fourth diode connected in series between the signal wire and a second power supply, connected so that ~~in a way~~ a current flows from the second power supply to the signal wire via the third and fourth diodes; and

a first capacitor and a second buffer amplifier connected in series between an output terminal of the first buffer amplifier ~~unit~~ and a first junction point of the first diode and the second diode;

a first resistor connected to a junction point of the first capacitor and the second buffer amplifier ~~unit~~ and connected to a point ~~having~~ maintained at a voltage, the value of which is between a voltage of
the first power supply and a voltage of the signal wire;

a second capacitor and a third buffer amplifier connected in series between the output terminal of the first buffer amplifier ~~unit~~ and a second junction point of the third diode and fourth diode;

a second resistor connected to a junction point of the second capacitor and the third buffer amplifier ~~unit~~ and to a point ~~having~~ maintained at a voltage, the value of which is between a voltage of the second power supply and the voltage of the signal wire; and

a third resistor connected between the signal wire and a voltage maintained at a value that is equal to or lower than the voltage of the first power supply, and equal to or higher than the voltage of the second power supply.

12. (Original) A method that detects capacitance of a capacitor ~~to be detected~~, comprising:

connecting the capacitor to be detected and an input of a first buffer amplifier ~~unit,~~ wherein the voltage gain of the first buffer amplifier is unity, ~~of which voltage gain is 1~~ via a signal wire;

connecting a first diode and a second diode in series between the signal wire and a first power supply and connecting a third diode and a fourth diode in series between the signal wire and a second power supply; and

canceling capacitance of the first diode and the third diode connected to the signal wire by connecting an output terminal of the buffer amplifier to a junction

point of the first diode and the second diode via a first capacitance and to a junction point of the third diode and the fourth diode via a second capacitance;

wherein the first junction point is connected to a point ~~having~~ maintained at a voltage, the value of which is between a voltage of the first power supply and a voltage of the signal wire, via a first resistor; and

the second junction point is connected to a point ~~having~~ maintained at a voltage, the value of which is between a voltage of the second power supply and the voltage of the signal wire, via a second resistor.

14. The capacitance detection circuit according to claim 13, further comprising:

~~a~~ a first high pass filter connected between the first buffer amplifier ~~unit~~ and the first junction point; and

a second high pass filter connected between the first buffer amplifier ~~unit~~ and the second junction point,

wherein the first high pass filter and the second high pass filter pass frequency elements corresponding to an AC voltage outputted from the AC power supply and to varying ~~variant~~ capacitance of the capacitor for detection, wherein the frequency elements are included in a signal outputted from the first buffer amplifier ~~unit~~.

15. (New) The capacitance detection circuit according to claim 8,

wherein the testing capacitor, the switch, and the first buffer amplifier ~~unit~~ are connected so that the ~~testing~~ capacitor to be detected can be connected, via the switch, between the input terminal and the output terminal of the first buffer amplifier ~~unit~~.

2. The following is an examiner's statement of reasons for allowance:

Taylor (US Patent Application Publication US 2007/0074988 A1) discloses a capacitive test point voltage and phasing detector, in which a method and apparatus for determining the presence of voltage at capacitive test points and determining the phase angle between two capacitive points is disclosed. The phase angle is determined based

on the actual phase angle difference between the voltage waveforms at the capacitive test points.

Takekawa et al. (US Patent Application Publication US 2006/0017449 A1) discloses a circuit for detecting difference in capacitances, in which an oscillator and phase comparator output a signal responsive to a phase difference between a delay caused by the first and second capacitances, and an integration circuit outputs a signal produced by integrating the phase difference signal over a time period equal to a predetermined number of cycles of the oscillator signal, coupled to a sample and hold circuit.

Lalla (US Patent Application Publication US 2005/077909 A1) discloses a circuit configuration for a capacitive sensor, using a reference capacitor and a buffer amplifier coupled to a measuring capacitor. At the beginning of each measurement cycle, the measuring capacitor is discharged to a predetermined residual charge, and the reference capacitor is charged to a predetermined reference charge, and the charge on the reference capacitor is then transferred to the measuring capacitor, and a capacitance of the measuring capacitor is determined.

Denen et al. (US Patent Application Publication US 2004/0160234 A1) discloses a proximity detection circuit and method of detecting capacitance changes, in which a balanced bridge circuit is used to detect a phase difference, which depends on the amount of detected capacitance difference or change of capacitance in a region of detection.

Tagg et al. (US Patent Application Publication US 2003/0067451 A1) discloses capacitive touch sensors, in which means for reducing noise effects, means to

approximate impedances and at least two multiplexers are included in the disclosed apparatus. A synchronous demodulator is used as a tracking filter to track the frequency of a capacitance measuring signal from one to the other of the sensor pads. A controller is also disclosed, connected to a number of pads or capacitive detection zones by way of buffered multiplexers and shielded connectors and cables.

Lambert et al. (US Patent Application Publication US 2002/0154039 A1) discloses a capacitive proximity sensor in which housing includes a first and second set of electrodes, interdigitally spaced from each other, and a ground electrode made from a flexible metallic braid. A synchronous detector is used to detect a phase shift caused by a sensed capacitance, relative to a reference signal.

Takekawa et al. (US Patent 7,250,773 B2) discloses a circuit for detecting difference in capacitances, in which an oscillator and phase comparator output a signal responsive to a phase difference between a delay caused by the first and second capacitances, and an integration circuit outputs a signal produced by integrating the phase difference signal over a time period equal to a predetermined number of cycles of the oscillator signal, coupled to a sample and hold circuit. In some embodiments, a first and second oscillator is disclosed, with first and second counters coupled to the oscillators, and the difference in capacitances is indicated by a difference between a first and second count in the first and second counters.

Lambert (US Patent 6,724,324 B1) discloses a capacitive proximity sensor in which housing includes a first and second set of electrodes, and a grounded middle electrode with a conductive surface situated between the first and second electrodes. A

synchronous detector is used to detect a capacitance change due to proximity of an object.

McIntosh et al. (US Patent 6,456,477 B1) discloses a linear capacitance detection circuit in which a differential transconductance amplifier detects changes of a variable capacitance in a low impedance bridge circuit, and feeds back current to balance the bridge. The voltage that controls the feedback current is proportional to capacitance over a wide dynamic range. Also disclosed is the use of a ratiometric bridge-like network that detects small differences in capacitance between a variable sensing capacitor and a fixed, stable reference capacitor, or alternatively, between two variable capacitors.

However, as to claim 1, the prior art of record fails to teach or suggest, singly or in combination, a capacitance detection circuit including:

The first junction point is connected to a point having a voltage whose value is between the voltage of the first power supply, and the voltage of the signal wire, via a first resistor

and

The second junction point is connected to a point having a voltage whose value is between the voltage of the second power supply and the voltage of the signal wire, via a second resistor

in combination with the other elements of independent claim 1.

Dependent claims 1, 4 – 8, 13 – 15, definite and enabled by the specification, are also allowed due to their dependence on independent claim 1.

As to claim 9, the prior art of record fails to teach or suggest, singly or in combination, a circuit that detects a capacitance of a capacitor including:

The first junction point is connected to a point having a voltage, the value of which is between the voltage of the first power supply and the voltage of the signal wire, via a first resistor

and

The second junction point is connected to a point having a voltage, the value of which is between the voltage of the second power supply and the voltage of the signal wire, via a second resistor

in combination with the other elements of independent claim 9.

As to claim 10, the prior art of record fails to teach or suggest, singly or in combination,

a circuit that detects a capacitance of a capacitor including:

A resistor connected to the first junction point and to a point maintained at a voltage, the value of which is between the voltage of the first power supply and the voltage of the signal wire

and

A resistor connected to the second junction point and to a point maintained at a voltage, the value of which is between the voltage of the second power supply and the voltage of the signal wire

in combination with the other elements of independent claim 10.

As to claim 11, the prior art of record fails to teach or suggest, singly or in combination,

a capacitance detection circuit including:

A second resistor connected to a junction point of the second capacitor and the third buffer amplifier and to a point maintained at a voltage, the value of which is between a voltage of the second power supply and the voltage of the signal wire;

and

A third resistor connected between the signal wire and a voltage maintained at a value that is equal to or lower than the voltage of the first power supply, and equal to or higher than the voltage of the second power supply.

in combination with the other elements of independent claim 11.

As to claim 12, the prior art of record fails to teach or suggest, singly or in combination, a method that detects capacitance of a capacitor, including:

The first junction point is connected to a point maintained at a voltage, the value of which is between a voltage of the first power supply and a voltage of the signal wire, via a first resistor;

and

The second junction point is connected to a point maintained at a voltage, the value of which is between a voltage of the second power supply and the voltage of the signal wire, via a second resistor.

in combination with the other elements of independent claim 12.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin M. Baldridge whose telephone number is 571 270 1476. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571 272 2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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